WHAT IS CLAIMED IS:

1. A thin film magnetic memory device for writing K-bit write data in parallel (where K is an integer of at least 2), comprising:

a plurality of memory cells arranged in a matrix, and each having an electric resistance according to storage data magnetically written therein;

a plurality of write digit lines arranged respectively corresponding to the memory cell rows, for passing therethrough a prescribed write current of a fixed direction in a selected row in data write operation;

a plurality of bit lines arranged respectively corresponding to the memory cell columns, for passing therethrough a data write current of a direction according to a level of said write data;

at least K current return lines each for turning back said data write current flowing through one of K selected bit lines of K columns selected to write said K-bit write data as necessary; and

a write driver for supplying said data write current to said K selected bit lines in directions respectively corresponding to said K-bit write data, wherein

said write driver connects said K selected bit lines and L of said current return lines in series between first and second voltages in said data write operation (where L is an integer in a range of 0 to K).

2. The thin film magnetic memory device according to claim 1, wherein

each of said current return lines is provided for each of said K selected bit lines,

said write driver includes

first switch provided corresponding to each of said K selected bit lines and connected between one end of a corresponding selected bit line and one end of a corresponding one of said current return lines, and

second switch provided corresponding to each of said K selected bit lines and connected between the other end of said corresponding selected bit line and the other end of said corresponding one

of said current return lines, and

when bits of said write data respectively corresponding to i^{th} and $(i + 1)^{th}$ ones of said K selected bit lines have a same level (where i is an integer in a range of 1 to (K – 1)), one of said first and second switch corresponding to the i^{th} selected bit line is selectively turned ON.

3. The thin film magnetic memory device according to claim 1, wherein

said write driver includes

a first switch connected between one ends of every adjacent two bit lines among said K selected bit lines, and

a second switch connected between the other ends of every adjacent two bit lines among said K selected bit lines, and

when bits of said write data respectively corresponding to i^{th} and $(i + 1)^{th}$ ones of said K selected bit lines have different levels (where i is an integer in a range of 1 to (K – 1)), one of said first and second switch between the i^{th} and $(i + 1)^{th}$ selected bit lines is selectively turned ON.

4. The thin film magnetic memory device according to claim 1, wherein

said write driver includes

first and second switches respectively provided between said first voltage and both ends of a first one of said K selected bit lines, and

third and fourth switches respectively provided between said second voltage and both ends of a K^{th} one of said K selected bit lines,

one of said first and second switch is turned ON according to a bit of said write data corresponding to said first selected bit line, and

one of said third and fourth switch is turned ON according to a bit of said write data corresponding to said K^{th} selected bit line.

5. The thin film magnetic memory device according to claim 1, wherein when bits of said write data respectively corresponding to i^{th} and $(i + 1)^{th}$ ones of said K selected bit lines have a same level (where i is an

integer in a range of 1 to (K – 1)), a data write current flowing through the i^{th} selected bit line is turned back by the current return line corresponding to the i^{th} selected bit line and then transmitted to the $(i + 1)^{th}$ selected bit line.

6. The thin film magnetic memory device according to claim 1, wherein said current return lines are formed in a wiring layer different from that of said plurality of bit lines.

7. The thin film magnetic memory device according to claim 6, wherein said current return lines are formed in a layer located above said plurality of bit lines.

8. The thin film magnetic memory device according to claim 1, wherein

said current return lines are formed in a wiring layer different from that of said plurality of bit lines,

each of said memory cells includes

a magneto-resistance element having an electric resistance according to said storage data, and

an access element electrically coupled between a corresponding one of said bit lines and one of said current return lines in series with said magneto-resistance element, and selectively turned ON in data read operation, and

each of said current return lines is coupled to a predetermined voltage in said data read operation.

9. A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, each memory cell having an electric resistance that varies according to storage data magnetically written therein;

a plurality of write digit lines arranged respectively corresponding to the plurality of memory cell rows, for passing therethrough a prescribed

current of a fixed direction in a selected row in data write operation;

a plurality of bit lines arranged respectively corresponding to the plurality of memory cell columns for passing therethrough a data write current of a direction corresponding to a level of write data in a selected column in said data write operation;

first and second write current control lines respectively provided at both ends of said plurality of bit lines so as to extend in a direction along said memory cell rows, and shared by said plurality of bit lines;

a first connection control portion for connecting one of said first and second write current control lines to a first voltage in said data write operation;

a second connection control portion for connecting the other of said first and second write current control line to a second voltage in said data write operation;

a plurality of column selection lines arranged respectively corresponding to said plurality of memory cell columns, and activated in a selected column; and

write drivers provided respectively corresponding to said memory cell columns, and each connecting a corresponding one of said bit lines between said first and second write current control lines, in response to activation of a corresponding one of said plurality of column selection lines.

10. The thin film magnetic memory device according to claim 9, wherein each of said write drivers includes

a first bit line drive switch provided between one end of said corresponding one of said bit lines and said first write current control line, and turned ON in response to activation of said corresponding one of said column selection lines, and

a second bit line drive switch provided between the other end of said corresponding one of said bit lines and said second write current control line, and turned ON in response to activation of said corresponding one of said column selection lines.

11. The thin film magnetic memory device according to claim 9, wherein said first and second connection control portions control connection between said first and second write current control lines and said first and second voltages according to a level of said write data.

12. The thin film magnetic memory device according to claim 9, wherein

said memory array is divided along a direction of said memory cell rows into a plurality of memory blocks,

in each memory cell column, said bit line is divided by said plurality of memory blocks,

said write drivers are provided respectively corresponding to said memory cell columns in each memory block,

said first and second write current control lines and said first and second connection control portions are provided for each memory block, and

each of said column selection lines is shared by said plurality of memory blocks.

13. The thin film magnetic memory device according to claim 12, wherein, in said data write operation, said first and second connection control portions corresponding to a non-selected memory block connect corresponding first and second write current control lines to a lower one of said first and second voltages.

14. The thin film magnetic memory device according to claim 9, wherein

said thin film magnetic memory device writes K-bit write data in parallel (where K is an integer of at least 2),

said memory array is divided into K sub blocks (first to K^{th} sub blocks) along a direction of said memory cell columns (where K is an integer of at least 2), said K sub blocks respectively corresponding to the K bits of said write data,

said first and second write current control lines are divided by said K

sub blocks,

said first connection control portion connects one of first and second write current control lines corresponding to the first sub block to said first voltage, and

said second connection control portion connects one of first and second write current control lines corresponding to the K^{th} sub block to said second voltage,

said thin film magnetic memory device further comprising:

a current direction regulating circuit provided between every adjacent two sub blocks, for controlling connection between first and second write current control lines corresponding to one of said adjacent two sub blocks and first and second write control lines corresponding to the other of said adjacent two sub blocks, wherein

said current direction regulating circuit between i^{th} and $(i + 1)^{th}$ sub blocks controls a direction in which a data write current flowing across said i^{th} sub block is transmitted to said $(i + 1)^{th}$ sub block according to a comparison result of i^{th} and $(i + 1)^{th}$ bits of said write data (where i is an integer in a range of 1 to $(K - 1)$).

15. The thin film magnetic memory device according to claim 14, wherein, when said i^{th} and $(i + 1)^{th}$ bits of said write data have a same level, said current direction regulating circuit between said i^{th} and $(i + 1)^{th}$ sub blocks either connects a first write current control line corresponding to said i^{th} sub block to a second write current control line corresponding to said $(i + 1)^{th}$ sub block, or connects a second write current control line corresponding to said i^{th} sub block to a first write current control line corresponding to said $(i + 1)^{th}$ sub block, according to said i^{th} and $(i + 1)^{th}$ bits.

16. The thin film magnetic memory device according to claim 14, wherein, when said i^{th} and $(i + 1)^{th}$ bits of said write data have different levels, said current direction regulating circuit between said i^{th} and $(i + 1)^{th}$ sub blocks either connects a first write current control line corresponding to

said i^{th} sub block to a first write current control line corresponding to said $(i + 1)^{th}$ sub block, or connects a second write current control line corresponding to said i^{th} sub block to a second write current control line corresponding to said $(i + 1)^{th}$ sub block, according to said i^{th} and $(i + 1)^{th}$ bits.

17. The thin film magnetic memory device according to claim 14, wherein, when said i^{th} and $(i + 1)^{th}$ bits of said write data have a same level, said current direction regulating circuit between said i^{th} and $(i + 1)^{th}$ sub blocks turns back a data write current flowing across said i^{th} sub block to transmit said data write current to said $(i + 1)^{th}$ sub block.

18. A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, each memory cell having an electric resistance that varies according to storage data magnetically written therein, said memory array being divided into a plurality of memory blocks along a direction of the memory cell rows; and

a plurality of write digit lines arranged respectively corresponding to said plurality of memory cell rows, for passing therethrough a prescribed write current of a fixed direction in a selected row in data write operation;

a plurality of bit lines arranged respectively corresponding to the plurality of memory cell columns, wherein in each memory cell column, said bit line is divided by said plurality of memory blocks,

said thin film magnetic memory device further comprising:

a plurality of column selection lines arranged respectively corresponding to said plurality of memory cell columns, for transmitting a column selection result, each column selection line being shared by said plurality of memory blocks; and

a plurality of write drivers provided respectively corresponding to said plurality of bit lines, and each operating in response to activation of a corresponding one of said plurality of column selection lines to supply a data write current of a direction corresponding to a level of write data to a corresponding one of said plurality of bit lines.